

REMARKS

As a preliminary matter, applicant appreciates the examiner's indication in the advisory action that claims 1, 2, 5-10, and 12 are allowed.

The examiner maintains his rejection of claims 3, 4, and 11 under 35 U.S.C. §102(b) as being anticipated by Shimomaki (U.S. Pub. No. 2002/0057243). Applicant traverses the rejection for the reasons listed below.

Regarding claim 3, applicant traverses the rejection because Shimomaki fails to disclose that a value of an on-voltage of a gate signal in the pre-scanning is different from a value of an on-voltage of a gate signal in the main scanning.

The examiner asserts that this feature is shown in Fig. 2A of Shimomaki because the values V1 and V2 are not the same. However, voltages V1 and V2 do not represent an on-voltage of a gate signal. Instead, as disclosed in paragraph [0059], V1 and V2 represent field-through voltages. The field-through voltages measure a drop in the liquid crystal application voltage that occurs when a scanning signal drops (see paragraph [0012]). Shimomaki does disclose a scanning signal Vg that is similar to the gate signal as recited in claim 3, but as shown in Fig. 2A, the signal Vg has identical values during period Ta and Tb. Thus, because Shimomaki fails to disclose a value of an on-voltage of a gate signal in the pre-scanning that is different from a value of an on-voltage in the main scanning, withdrawal of the rejection of claim 3 is respectfully requested.

With respect to claim 4, applicant traverses the rejection because Shimomaki fails to disclose a length between timing of raising of a gate signal and the timing of the next

following breaking down of the gate signal and the pre-scanning period is different from that in the main scanning period.

The examiner asserts that Shimomaki discloses this feature because the signal V_{sig} during period T_a (corresponding to gate pulse P1) is not the same as V_{sig} during period T_b (corresponding to gate pulse P2). However, V_{sig} is a display signal and not a gate signal. The scanning signal V_g of Shimomaki is more comparable to the gate signal recited in claim 4. However, as shown in Fig. 2A and described in paragraph [0067], the width (i.e., the timing between the raise and subsequent breaking down of signal V_g) of first and second gate pulses P1 and P2 are identical. Thus, Shimomaki fails to disclose that a length of time between the raising of a gate signal and the timing of the next following breaking down of the gate signal in the pre-scanning period is different from that in the main scanning period, as recited in claim 4. For this reason, applicant respectfully requests withdrawal of the rejection of claim 4.

Regarding claim 11, applicant traverses the rejection because Shimomaki fails to disclose that a value of a gate-off voltage between the pre-scanning period and the main scanning period is said to be higher than a value of the gate-off voltage after the main scanning period.


The examiner asserts that Fig. 2A of Shimomaki shows this feature because signal V_{p1} is higher between periods T_a and T_b than it is following period T_b . However, as disclosed in paragraph [0057] of Shimomaki, signal V_{p1} is a liquid crystal application voltage. That is, signal V_{p1} represents the voltage applied to the liquid crystal molecules

filled between the pixel electrode and the opposite electrode (see paragraph [0011]). Accordingly, signal Vp1 does not correspond to the gate voltage as recited in claim 11. Scanning signal Vg more closely corresponds to the gate signal recited in claim 11. However, as shown in Fig. 2A, the value of scanning signal Vg between periods Ta and Tb is identical to the value of signal Vg after period Tb. Accordingly, Shimomaki fails to disclose that a value of a gate-off voltage between the pre-scanning period and the main scanning period is higher than the value of the gate-off voltage after the main scanning period. For this reason, applicants respectfully request withdrawal of the rejection of claim 11.

If a Petition under 37 C.F.R. §1.136(a) for an extension of time for response is required to make the attached response timely, it is hereby petitioned under 37 C.F.R. §1.136(a) for an extension of time for response in the above-identified application for the period required to make the attached response timely. The Commissioner is hereby authorized to charge fees which may be required to this application under 37 C.F.R. §§1.16-1.17, or credit any overpayment, to Deposit Account No. 07-2069.

For the foregoing reasons, applicant believes that this case is in condition for allowance, which is respectfully requested. The examiner should call applicant's attorney if an interview would expedite prosecution.

Respectfully submitted,
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